Meniscus-Mask Lithography for Narrow Graphene Nanoribbons

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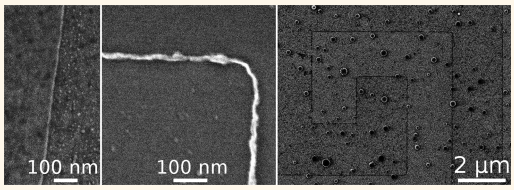
ABSTRACT Described here is a planar top-down method for the fabrication of precisely positioned very narrow (sub-10 nm), high aspect ratio (>2000) graphene nanoribbons (GNRs) from graphene sheets, which we call meniscus-mask lithography (MML). The method does not require demanding high-resolution lithography tools. The mechanism involves masking by atmospheric water adsorbed at the edge of the lithography pattern written on top of the target material. The GNR electronic properties depend on the graphene etching method, with argon reactive ion etching yielding remarkably consistent results. The influence of the most common substrates (Si/SiO_2 and boron nitride) on the electronic properties of GNRs is demonstrated. The technique is also shown to be applicable for fabrication of narrow metallic wires, underscoring the generality of MML for narrow features on diverse materials.



KEYWORDS: graphene nanoribbons · meniscus-mask lithography · reactive ion etching · metallic wires

Fabrication of narrow, high aspect ratio objects allows both miniaturization and control of size-dependent properties of materials. The patterning of graphene[1] into sub-10 nm graphene nanoribbons (GNRs) results in objects that are expected to exhibit varied band gaps depending on the GNR width and edge configurations.[2,3] There are a number of GNR fabrication methods, including graphene patterning using various lithography methods,[4−6] shadowing techniques[7,8] including shadowing by copolymer masks,[9−11] processing of carbon nanotubes[12−14] and graphite,[15] growth on prepatterned substrates,[16,17] and direct organic synthesis.[18] However, only a few methods enable both scalable fabrication[19] and controlled narrow GNR positioning on-chip, characteristics that are currently required for industrial use in microelectronics. We disclose here a simple method to prepare sub-10-nm-wide GNRs by a top-down method called meniscus-mask lithography (MML).

RESULTS AND DISCUSSION

We demonstrate the MML GNR fabrication sequence in Figure 1A. In a typical process (Supporting Information Section S1), the lithography pattern is written on the graphene film in such a way that the desired GNR position corresponds to the pattern edge. After the pattern is developed, the exposed graphene is etched *via* reactive ion etching (RIE). A sacrificial metal layer is deposited, and the pattern is lifted off. Then the structure is once again exposed to RIE, and the sacrificial metal layer is wet-etched. As a result, the graphene near the initial pattern edges remains unaffected, and the process leads to the formation of narrow GNRs (Figure 1B−I, Supporting Information Section S2).

Two RIE regimes were tested for MML GNR fabrication: oxygen RIE, which is conventionally used for graphene etching,[4,20−22] and Ar RIE, which is milder since it removes graphene by physical sputtering only. The width was quite uniform over the ribbon length and between similarly fabricated samples (Supporting Information Section S3). For GNRs produced using oxygen RIE (ox-GNRs) on Si/SiO_2 and boron nitride (BN) substrates, the mean widths were 13.6 ± 1.0 nm and 14.2 ± 1.0 nm, respectively. For GNRs produced using Ar RIE (ar-GNRs) the widths were smaller, 8.7 ± 1.0 nm and 6.4 ± 1.0 nm for Si/SiO_2 and BN substrates, respectively. The resulting GNRs demonstrated remarkably high aspect ratios (>2000), limited predominantly by the macroscopic defects in the original transferred graphene film.

The method described could also be expanded to other materials. We have substituted graphene with sputtered 15 nm

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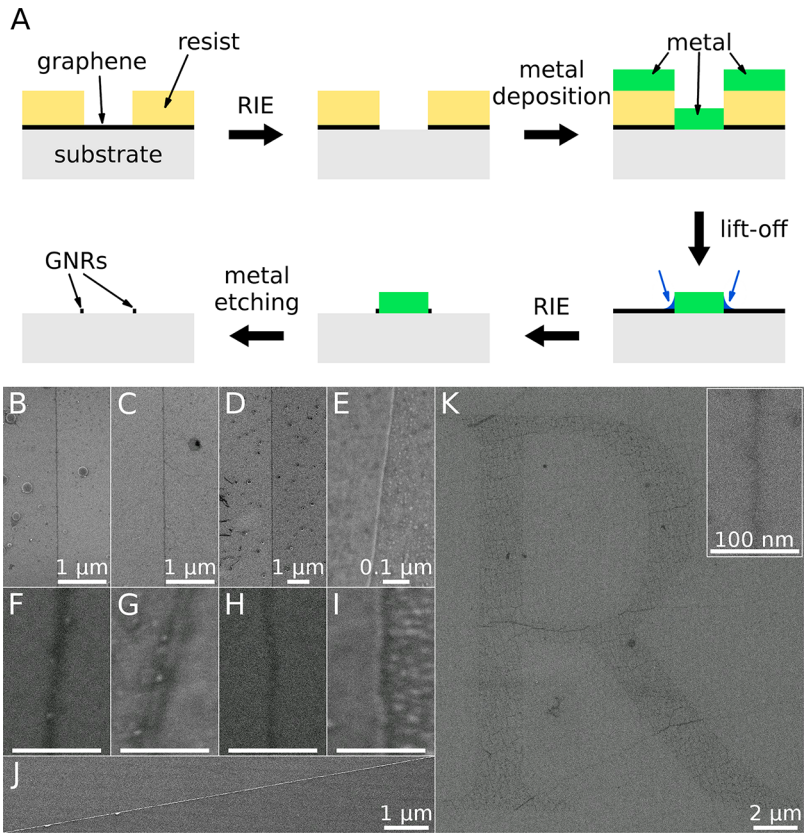

Figure 1. MML fabrication. (A) MML GNR fabrication scheme. Formation of GNRs occurs at the edge of the lithography pattern. Blue arrows point to the meniscus of the adsorbed water, which serves as the mask for the ultimate GNRs. (B–I) SEM images of individual GNRs at different magnifications. (B and F) ox-GNRs on Si/SiO_2; (C and G) ox-GNRs on BN; (D and H) ar-GNRs on Si/SiO_2; (E and I) ar-GNRs on BN. The scale bar for images (F)–(I) is 100 nm. (J) Pt wire on Si/SiO_2. (K) The letter R patterned with ar-GNRs. The GNRs are only at the inner and outer edges of the letter R. Inset: Magnified image of a part of the ar-GNR comprising the letter R. The mean width is 9.2 ± 1.1 nm.

platinum films, and a similar fabrication sequence resulted in platinum nanowires with mean width 11.7 ± 1.0 nm (Figure 1J, Supporting Information Sections S4, S5).

The GNRs can be fabricated by MML in different shapes (Figure 1K, Supporting Information Section S6) with the only limitation being that they are located on the edge of the written pattern; the GNR width does not depend on the pattern shape. Note that the fabrication resulted in identical GNRs on all sides of the pattern, thus excluding shadowing due to sample tilt during RIE as a possible formation mechanism.

The GNR widths are robust over a range of the lithography dosages used (Supporting Information Section S7). They do not depend on the sacrificial metal used in the fabrication: the GNR widths for Pd, Pt, and Al were nearly the same. Thus, the formation of the GNRs does not depend on the ability of the metal to form a native oxide layer, and the mechanism is not related to oxide layer shadowing.[19] Also, GNR widths remained nearly the same for different Al layer thicknesses (Supporting Information Section S8).

We propose that MML works for GNR formation by adsorbate protection (shown by blue arrows in Figure 1A) of the graphene surface during the second RIE step. The adsorbate is most likely atmospheric water, confined to the wedge formed by the graphene and sacrificial metal. Such adsorbates could be stabilized by concave surface features (pores, wedges) and could sustain short low-pressure procedures such as RIE. The mechanism was experimentally supported by the fact that no GNRs were formed when the sample was heated to 120 °C for 30 min prior to etching nor when the sample was soaked in acetone prior to etching to ensure no contact with atmospheric moisture (Supporting Information Section S9). The meniscus in the wedge formed by the substrate and sacrificial metal mask is too small to be described with continuum models (Supporting Information Section S10.1); however, we show that a few-layer-thick adsorbate beading near the pattern edge could be explained using a simple first-order approximation molecular model of adsorption (Supporting Information Section S10.2). This few-layer meniscus has a size comparable to the width of observed GNRs and likely protects the underlying graphene area from RIE. Note that for MML the resolution is determined by the shape of the liquid meniscus; this might be controlled with the judicious choice of solvent or substrate treatment, enabling width variations in the final masked object.

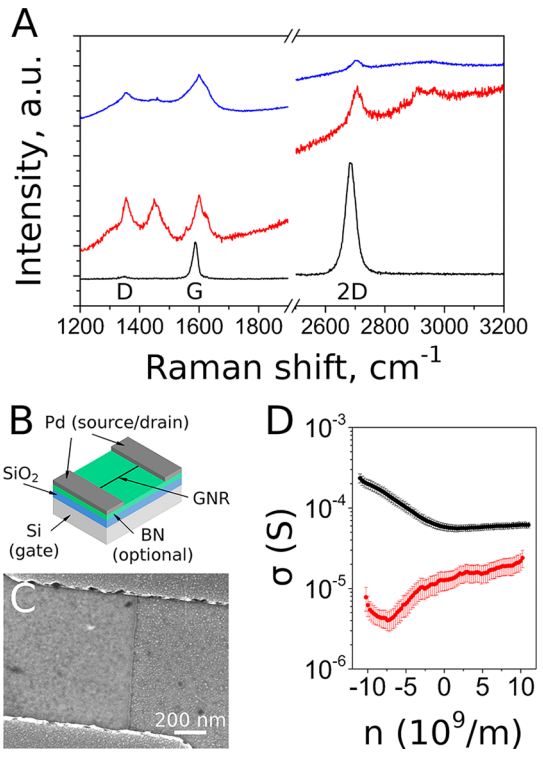

Figure 2. Raman spectra and room-temperature transport measurements of GNRs. (A) Raman spectra: ar-GNR on Si/SiO_2 in blue (top), ox-GNR on Si/SiO_2 in red (middle), and the starting CVD graphene in black (bottom). The spectra are normalized so that the G peak height is approximately the same for all three spectra. (B) Scheme of the device used for transport measurements. (C) SEM image of an ar-GNR device on a BN substrate. The GNR is situated vertically between the horizontal top and bottom electrodes. (D) Room-temperature gating curves (for source−drain voltage 0.1 V) for individual ar-GNR FETs on Si/SiO_2 (in black) and BN (in red) substrates. σ is the planar conductivity and n is the linear charge carrier concentration (positive for electrons).

Since the GNRs are formed at the edge of the pattern, the procedure does not require lithography setups to have very high resolution. Thus, similar fabrication procedures could be performed even with photolithography (Supporting Information Section S11). The GNR mean width of 23 ± 4 nm was slightly higher than for GNRs fabricated using the e-beam lithography procedure. To our knowledge, this is first time that narrow GNRs have been fabricated by photolithography.

Raman spectra of GNRs (Figure 2A) revealed characteristic 2D (~2700 cm^{-1}), G (~1584 cm^{-1}), and D (~1350 cm^{-1}) peaks for both ox-GNRs and ar-GNRs on Si/SiO_2 substrates. The G/2D intensity ratio for the GNRs increases as the GNR widths decrease: for undoped graphene the G/2D ratio is ~0.3 (ref 23), whereas it is 1.0 ± 0.2 and 4.3 ± 0.5 for ox-GNRs and ar-GNRs, respectively, which is likely attributed to intrinsic GNR properties.[24] In all GNR spectra, the G peak is considerably wider compared to that of the starting CVD graphene film, as expected for narrow GNRs;[24] interestingly, for ar-GNRs the wide G peak could be interpreted as a doublet (Supporting Information Section S12).

The ar-GNRs are narrower than ox-GNRs; hence they might have a larger edge-effect. However, the D/G intensity ratio for ar-GNRs is lower (0.6 ± 0.1) than for ox-GNRs (1.1 ± 0.1), indicating that oxygen RIE leaves GNRs more disordered compared to Ar RIE. Assuming the protective adsorbates mechanism, the difference is likely caused by more defects in the narrow region near the edges for ox-GNRs compared to ar-GNRs.

To investigate the electronic properties of narrow GNRs, field-effect transistor (FET) devices were fabricated (Figure 2B,C) with Pd source and drain electrodes placed on the ribbons and a 300 nm thermal oxide coated p^{++}-Si substrate used as a back gate. The channel length was 0.8 to 3.5 μm. For each type of GNR at least 12 devices were studied (Supporting Information Section S13). The Si/SiO_2 substrate is known to cause electron and hole puddles in graphene, resulting in charge-trapping effects.[25] The conventional method to avoid charge trapping in graphene devices is to use a BN flake as the substrate;[25,26] the charge-trapping effects due to Si/SiO_2 have been demonstrated in GNRs.[27] ar-GNR devices on both Si/SiO_2 and BN substrates (30 to 70 nm thick) demonstrated remarkably consistent behavior (Figure 2D). Room-temperature gating curves in Figure 2D were averaged over 50 devices for Si/SiO_2 and over 12 devices for BN substrates, and the conductivity was calculated using the widths of the GNRs as 8.7 nm on Si/SiO_2 and 6.4 nm on BN. In contrast to ar-GNRs, wider ox-GNRs on Si/SiO_2 substrates had strong variation in both ON/OFF ratios and charge neutrality point positions, while ox-GNRs on BN substrate had a consistent charge neutrality point position, but still large ON/OFF variation (Supporting Information Section S13). Interestingly, the room-temperature ON/OFF ratio for ar-GNRs is rather modest, ~10. This contrasts with some reports on the electronic behavior of similarly narrow or even larger width GNRs that showed extremely high ON/OFF ratios (up to 10^7) observed at room temperature.[15] We have estimated the hole mobility as ~14 $cm^2/V \cdot s$ for ar-GNRs on Si/SiO_2 substrate, which agrees well with published data on charge carrier mobilities in narrow GNRs.[11,17] When discussing the electronic properties of GNRs with defective edges, it is important to distinguish the true band gap[2,3] from the so-called transport or mobility gap that originates from Coulomb blockade due to edge defects[20−22,28] or substrate-induced alternating electron and hole puddles.[27] Both BN and Si/SiO_2 substrates result in potential fluctuations over the GNR length; however, the lateral scale and the amplitude of those strongly differ. For Si/SiO_2, the characteristic size of the puddle is much smaller and the fluctuations of potential amplitude much higher compared to BN.[25]

According to the Raman spectral data, ar-GNR edges are less defective compared to ox-GNRs. The Si/SiO_2 substrate induces potential fluctuations that are comparable with fluctuations caused by edge defects in

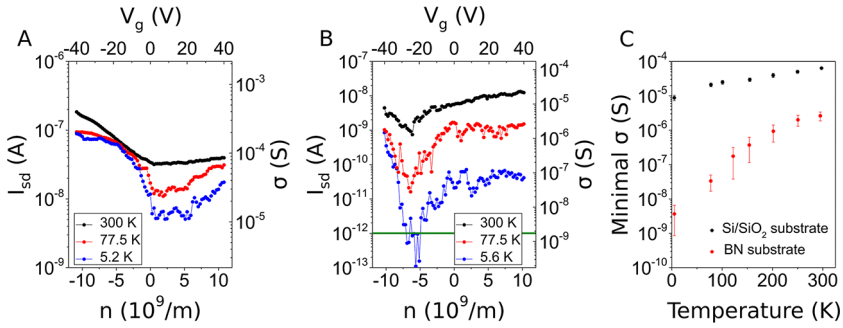

Figure 3. Temperature-dependent electronic properties for typical ar-GNR FETs. Gating curves at different temperatures for GNR FETs on (A) Si/SiO_2 substrate or (B) BN substrate. The green line at 10^{-12} A in (B) depicts the approximate instrument noise level. The source−drain voltage was 0.1 V. I_{sd} is source−drain current, V_g is gate voltage, σ is planar conductivity, and n is linear charge carrier concentration (positive for electrons). (C) Temperature dependence of minimal conductivity averaged for six devices for each substrate type.

ox-GNRs (Supporting Information Section S13), while they dominate over potential fluctuations caused by edge defects in ar-GNRs; the electronic properties of ar-GNRs on Si/SiO_2 are determined predominantly by substrate interactions. In the case of the ar-GNRs on BN substrates, both potential fluctuations due to the edge defects and substrate interaction are rather small. Since the ON/OFF ratio for ar-GNRs on BN is comparable to that observed for ar-GNRs on Si/SiO_2 substrates, it is likely that the true band gap is dominating the behavior of ar-GNRs on the BN substrate (Supporting Information Section S13). The band gap for the ar-GNRs could be estimated from theoretical studies.[2] Accordingly, a 6.4-nm-wide zigzag-edged GNR yields an expected band gap of ∼0.12 eV. Band-gap estimation for armchair-edged GNRs is more difficult since the properties of ideal armchair GNRs differ strongly depending on the number of dimer lines in the GNR structure.[2] Band-gap E_g dependence on GNR width w could be summarized[20] as $E_g = a/w$, where the coefficient a takes values between 0.2 and 1.5 eV·nm. This, indeed, could exceed the potential fluctuations due to the BN substrate.[25]

Low-temperature transport properties of ar-GNRs on Si/SiO_2 and BN are shown in Figure 3. For ar-GNRs on Si/SiO_2 (Figure 3A), upon cooling from room temperature to 5 K, the ON/OFF ratio increased only from ∼4 to ∼20, and the gating curves demonstrate, especially at 200 K and below, a clear plateau for low currents that is significantly above the measurement limit of the instrument. The plateau observed could be interpreted in terms of a transport gap.[20−22,28] Apparently, the source−drain voltage is high enough so that for all gate voltages corresponding to Coulomb blockade the barrier size is small, which results in measurable tunneling current. The small change in minimal conductivity with temperature agrees with this conclusion and is consistent for all devices measured (Figure 3C).

The gating curves for ar-GNRs on BN substrate are quite different. The lowest current (OFF) decreases about 3 orders of magnitude upon cooling from 300 K to 5 K; near the temperature of liquid helium it reaches the noise level (Figure 3B, green line). The ON/OFF ratio for ar-GNRs on BN thus increases from ∼10 to ∼10^3, which, together with the current dropping to a minimal measurable value, agrees with the presence of a true band gap.[4]

CONCLUSIONS

In conclusion, we have demonstrated a scalable top-down method for fabrication of high aspect ratio narrow objects by means of simple lithography that we termed MML and showed its applicability to prepare very narrow GNRs of arbitrary configuration. The apparent formation mechanism is graphene protection by adsorbates in the wedge formed by the sacrificial metal layer and the graphene on the edge of the lithography pattern. The Ar RIE process was found to result in fabrication of GNRs with consistent electronic properties. The ar-GNR on Si/SiO_2 behavior could be explained in terms of the transport gap, while the electronic properties of ar-GNRs on BN substrate could be explained by the presence of a true band gap.

METHODS

Fabrication of GNRs was performed using CVD graphene as the starting films (Supporting Information Section S1). Fabrication of platinum wires was performed starting from a 15 nm thick platinum film sputtered on the substrate using a Denton Desk V Sputter system.

Room-temperature reactive ion etching with oxygen or argon was performed using a Trion RIE instrument and Oxford Plasma Lab 80 Plus RIE instrument. Varying temperature RIE processes with nitrogen were performed using a Trion Orion II Load Lock PECVD instrument. The conditions used are listed in the Supporting Information.

A sacrificial metal layer was deposited either by sputtering (Al and Pt, Denton Desk V Sputter system) or by e-beam evaporation (Pd). The sacrificial layer thickness was 20 nm unless stated otherwise. For Al wet etching the mixture of

$H_3PO_4/HNO_3/CH_3COOH/H_2O$ (80/5/5/10 vol %) was used.[29] Sacrificial Pt and Pd layers were etched using *aqua regia*.

GNR FET devices were fabricated *via* conventional e-beam lithography with 40 nm e-beam evaporated Pd pads. Electrical measurements were performed under vacuum (chamber pressure less than 10^{-5} Torr) using a Desert Cryogenic Probe 6 system. Prior to measurements the samples were held under vacuum for at least 4 d to ensure the desorption of atmospheric moisture from the GNRs. The *IV* data were recorded using an Agilent 4155C semiconductor parameter analyzer. Gate voltage was varied in the range −40 to +40 V; sweeping was performed from negative to positive voltages. For recording gating curves, the source−drain voltage was set to 0.1 V. Low-temperature measurements were performed in the range 5 to 300 K in the same system using a LakeShore 331 temperature controller with Si diode sensor.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Further details are provided on fabrication procedures, statistical analysis of GNR and nanowire width distributions, formation mechanism analysis, and Raman and electrical characterization. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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